Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

1. (currently amended) A semiconductor die package comprising:~~;~~

a semiconductor die;

a leadframe having a ~~chemically-etched~~ surface roughened by chemical-etching, an organo-metallic coating being formed on said chemically-etched surface; and

a capsule comprising a molding compound, said capsule enclosing at least a portion of said die and at least a portion of said leadframe, said molding compound being in contact with said organo-metallic coating on said chemically-etched surface ~~of said leadframe~~ so as to reduce the possibility of separation between said molding compound and said leadframe as said package undergoes thermal cycles and/or to inhibit the ingress of moisture into said package.

2. (original) The semiconductor package of Claim 1 wherein said leadframe consists essentially of copper alloy.

3-6. (canceled)

7. (previously presented) A semiconductor package comprising:

a semiconductor die;

a leadframe having a chemically-etched surface; and

a capsule enclosing at least a portion of said die and at least a portion of said leadframe;

said package further comprising an organo-metallic coating on the surface of the leadframe.

8-20. (canceled)

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21. (previously presented) The semiconductor package of Claim 1 wherein the arithmetic mean deviation of a profile of said chemically-etched surface is in the range of 0.050 µm to 0.170 µm.

22. (previously presented) The semiconductor package of Claim 21 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 µm to 0.700 µm.

23. (previously presented) The semiconductor package of Claim 22 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

24. (previously presented) The semiconductor package of Claim 21 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

25. (previously presented) The semiconductor package of Claim 24 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

26. (previously presented) The semiconductor package of Claim 22 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

27. (previously presented) The semiconductor package of Claim 21 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

28. (previously presented) The semiconductor package of Claim 1 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 µm to 0.700 µm.

29. (previously presented) The semiconductor package of Claim 28 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

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30. (previously presented) The semiconductor package of Claim 29 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

31. (previously presented) The semiconductor package of Claim 28 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

32. (previously presented) The semiconductor package of Claim 1 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

33. (previously presented) The semiconductor package of Claim 32 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

34. (previously presented) The semiconductor package of Claim 1 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

35. (canceled)

36. (previously presented) The semiconductor package of Claim 7 wherein the capsule is in contact with the organo-metallic coating so as to reduce the possibility of separation between said capsule and said leadframe as said package undergoes thermal cycles and/or to inhibit the ingress of moisture into said package.

37. (previously presented) The semiconductor package of Claim 1 wherein a recess is formed in the leadframe, a surface of the leadframe within the recess being chemically-etched.

38. (previously presented) The semiconductor package of Claim 1 comprising a plated metal layer on a portion of the leadframe.

39. (previously presented) The semiconductor package of Claim 38 wherein a surface of the leadframe under the plated metal layer is chemically-etched.

40. (previously presented) The semiconductor package of Claim 38 wherein a surface of the leadframe under the plated metal layer is not chemically-etched.

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41. (previously presented) The semiconductor package of Claim 1 wherein a top surface or a side surface of said leadframe is chemically-etched and a bottom surface of said leadframe is not chemically-etched.

42. (previously presented) The semiconductor package of Claim 1 wherein said chemically-etched surface is light brown to brown in color.

43. (previously presented) The semiconductor package of Claim 7 wherein the arithmetic mean deviation of a profile of said chemically-etched surface is in the range of 0.050 µm to 0.170 µm.

44. (previously presented) The semiconductor package of Claim 7 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 µm to 0.700 µm.

45. (previously presented) The semiconductor package of Claim 7 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

46. (previously presented) The semiconductor package of Claim 7 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

47. (previously presented) The semiconductor package of Claim 23 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

48. (new) The semiconductor package of Claim 1 wherein the roughened surface of the leadframe and the organo-metallic coating together reduce the possibility of separation between said molding compound and said leadframe as said package undergoes thermal cycles and/or inhibit the ingress of moisture into said package.

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